

Ryan Massie

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EDUCATION

Carnegie Mellon University

Master of Science in Electrical & Computer Engineering (ABET Accredited)

Pittsburgh, PA

Expected December 2027

Relevant Coursework: Digital Integrated Circuits, Embedded Systems, Nanofabrication, Hardware Verification.

Ohio Northern University

Bachelor of Science in Computer Engineering (GPA: 3.92/4.0, ABET Accredited)

Ada, OH

May 2025

WORK EXPERIENCE

Northrop Grumman Corporation

Software Engineering Intern

Beavercreek, OH

June 2022 - December 2025

- Summer 2022, Summer 2023, Summer 2024, Summer/Fall 2025
- Collaborated in a team to devise solutions for cycle-accurate real-time emulation via code generation, translated legacy ISA models into optimized C/C++ for x86, ARM, and RTOS platforms and compiled thorough documentation.
- Built and validated Motorola 68K and PPC ISA models, enabling execution of legacy mission-critical applications on modern hardware platforms.
- Implemented emulated peripheral devices by analyzing Hardware Reference Manuals and ISA documentation to recreate memory devices, system buses, I/O subsystems, and synchronization mechanisms.
- Led projects as a Scrum Master for an Agile team, improving sprint execution while remaining a core contributor.
- Replaced proprietary testing infrastructure with GoogleTest unit and functional tests, reducing annual costs by \$17K.

PUBLICATION

- "A High-Performance Hardware Design for Computing Bézout's Coefficients Using Extended Stein's Algorithm," IEEE International Conference on Electro/Information Technology (EIT), 2025. (Lead Author)

PROJECT EXPERIENCE

Sputtering Machine Automated Pressure Control System (Carnegie Mellon)

January 2026 - Present

- Developing novel designs for an automated argon pressure control embedded system for CMU Hacker Fab's custom sputtering machine, improving plasma stability and enabling precise material deposition onto target chips.

Binary GCD Hardware Research (Ohio Northern)

January 2024 – June 2025

- Spearheaded end-to-end design of a scalable 64-bit FPGA hardware architecture for computing Bézout's coefficients in cryptographic systems, including RTL development, verification, and hardware testing.
- Collaborated closely with a research advisor to communicate ideas, exchange feedback, and refine technical deliverables to produce a novel piece of research.
- Performed rigorous verification using self-checking test benches and automated regression testing for potential manufacturing by future student groups.

Capstone Micromouse Robot (Ohio Northern)

May 2024 – May 2025

- Organized a team of 5 engineers to deliver a high-performance IEEE Micromouse maze solving robot from scratch to compete at the IEEE Region 1/2 Student Conference, achieving at top finish.
- Engineered a real-time embedded system for sensor integration, motor control, and autonomous navigation; designed and fabricated custom PCBs to integrate with a Raspberry Pi. Tested assembly utilizing probes and oscilloscopes.

FPGA Hardware Accelerator (Ohio Northern)

January 2025 – March 2025

- Developed an external large-integer FPGA math accelerator interfaced with an ARM processor via AXI-Full to execute addition, subtraction, multiplication, and division of large integers.

SKILLS

Languages: *Advanced:* C/C++, CMake, Git; *Intermediate:* Python, Bash, GDB, ARM Assembly

Embedded and Hardware: *Advanced:* Embedded Linux, Firmware, Interrupts, I2C, UART; *Intermediate:* JTAG, AXI

VLSI/Design: *Advanced:* VHDL, Vivado; *Intermediate:* Computer Architecture, CPU Design, SystemVerilog, ModelSim

FPGA and Acceleration: *Intermediate:* RTL Design, Testbench Development, Timing Analysis

Electronics and Fabrication: *Intermediate:* Analog Circuits (Spice), PCB Design (Fusion), Soldering