Ryan Massie

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EDUCATION

Carnegie Mellon University — Pittsburgh, PA
Master of Science in Electrical & Computer Engineering (ABET Accredited) — *January 2026 - December 2027*

Ohio Northern University — Ada, OH
Bachelor of Science in Computer Engineering (ABET Accredited) — *August 2021 - May 2025*

- **GPA:** 3.92

EXPERIENCE

Northrop Grumman Corporation — June 2022 - December 2025
Software Engineering Intern — *Beavercreek, OH*

- Developed cutting-edge, real-time, cycle-accurate emulation technology utilizing code generation to convert legacy ISA models into C/C++ code, allowing legacy applications to run on modern x86/ARM hardware. Applied computer architecture and low-level programming expertise to develop accurate Motorola 68K ISA models for legacy system emulation.
- Collaborated as a Scrum Master within an Agile development team to enhance project efficiency and communication. Implemented a unit testing solution using GoogleTest, reducing costs by $17,000 annually compared to the previous proprietary solution.
- Redesigned the project build system using CMake to enable automatic dependency management and seamless integration between bare-metal and kernel-based applications, improving build efficiency and maintainability.
- Refactored shared emulation libraries for safe multi-process / multi-threaded execution (lock redesign: minimized hold times, increasing instruction efficiency by 7%.

T.J. Smull College of Engineering — January 2024—May 2025
Undergraduate Researcher — *Ada, OH*

- Served as lead author for a publication presented at the 2025 IEEE International Conference on Electro/Information Technology.
- Designed digital hardware to compute Bézout's coefficients for cryptographic applications using FPGAs, leveraging expertise in digital systems, VHDL, Verilog, and hardware testing.
- Enhanced department testing and peer review frameworks by creating automated scripts and standardized processes, improving code quality and reducing review time, enabling faculty to review additional reports & draft efficiently.

PROJECTS

Micromouse Robot

- Directed the design and development of an IEEE Micromouse competition robot, representing the team at the IEEE Region 1/2 Student Conference.
- Engineered a real-time embedded system for sensor integration, motor control, and autonomous navigation; designed and fabricated custom PCBs to support hardware functionality.
- Led a team of 5 engineers to deliver a high-performance robotic system optimized for competitive maze-solving, ensuring on-time project completion.

FPGA Hardware Accelerator

- Designed and implemented an FPGA-based audio processing system, enabling real-time filtering and signal analysis for advanced acoustic applications.
- Developed an external interrupt-driven hardware timer to provide precise, low-latency timing control and synchronization between FPGA logic and host system processes.
- Integrated the accelerator and timer into an existing ZedBoard, interfacing with processor cores and peripheral devices.

SKILLS

- **VLSI/Design:** VHDL, SystemVerilog, Vivado, Vitis, ModelSim, Computer Architecture, Digital Systems
- **Languages & Build:** C/C++, Python, Bash, CMake, ARM & RISC-V assembly
- **FPGA & Acceleration:** RTL Design, Testbench Development, Timing Analysis, Hardware/Software Co-Design
- **Embedded & Hardware:** ARM Cortex-M, Embedded Linux, Interrupt Handling, DMA, SPI, I2C, UART, JTAG
- **Lab & Fabrication:** PCB Design (Fusion), Soldering, Oscilloscope, Logic Analyzer